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In re Patent Application of
GENDRIER ET AL.
Serial No. **10/511,712**
Filed: **OCTOBER 15, 2004**

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REMARKS

Applicants thank the Examiner for the careful and thorough examination of the present application, for withdrawing the previous rejections and objections to the claims, and for indicating that dependent Claims 35-43, 45-66, 69-77, and 79-100 all recite patentable subject matter. Applicants submit that all claims are patentable and present arguments supporting such patentability below.

I. The Claimed Invention

Independent Claim 34 is directed to a semiconductor memory device comprising an electrically erasable and programmable non-volatile memory cell. The memory cell includes a layer of gate material and a floating-gate transistor including a floating gate, a source, a drain, and channel regions defining a control gate. The memory cell further includes a first active zone, a second active zone incorporating the control gate and electrically isolated from the first active zone, and a dielectric zone between a first part of the layer of gate material and the first active zone. The dielectric zone defines a transfer zone for transferring, during erasure of the memory cell, charges stored in the floating gate to the first active zone. Independent Claim 68 is a method counterpart to Claim 34.

II. The Claims Are Patentable

The Examiner rejected independent Claims 34 and 68 over the Patelmo et al. application. Patelmo et al. discloses a fabrication process for non-volatile memory cells with

salicided junctions. (Paragraph 1). The completed memory cell is depicted in Figure 23, reproduced below.

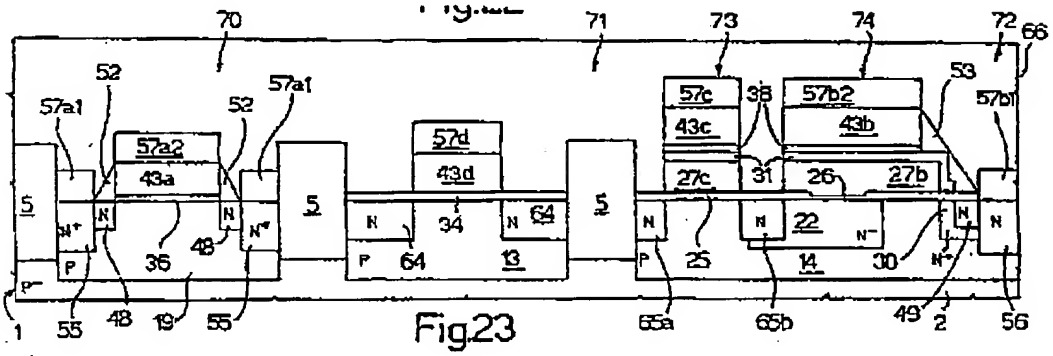

Figure 23 of the Patelmo et al. Application

The memory cell includes a dielectric layer **31** for electrically isolating the floating gate regions **27b** of adjacent memory cells. (Paragraphs 27-28). The Examiner cites the dielectric layer **31** of Patelmo et al. as disclosing a dielectric zone defining a transfer zone for transferring, during erasure of the cell, the charges stored in the floating gate to the first active zone, as recited in independent Claims 34 and 68.

Applicants respectfully submit that the Examiner has mischaracterized the dielectric layer **31** of Patelmo et al. Indeed, Patelmo et al. discloses that the dielectric layer **31** is "for electrically isolating the floating gate regions of adjacent cells." (Paragraph 28). The dielectric layer **31** does not define a transfer zone for transferring, during erasure of the cell, the charges stored in the floating gate as recited in independent Claims 34 and 68. Differently, the floating gate region **27b** of Patelmo et al. tunnels its charge

through the tunnel oxide region **26**. (Paragraphs 26 and 39). Therefore, for this reason alone, independent Claims 34 and 68 are patentable.

Moreover, the Examiner cited the active low voltage area **6** of Patelmo et al., as depicted in Figure 1, reproduced below, as disclosing the second active zone of the claimed invention. The control gate **43b** of Patelmo et al. is located adjacent the floating gate region **27b**. (Paragraph 39). The active low voltage area **6** cited by the Examiner forms the low voltage NMOS transistor **70** and not the memory transistor **74** and respective floating gate **27b**.

In contrast, independent Claims 34 and 68 recite a second active zone incorporating the control gate and electrically isolated from the first active zone. The active low voltage area **6** defines a low voltage NMOS transistor **7b** and not the control gate as in the claimed invention. Accordingly, for this reason also, independent Claims 34 and 68 are patentable.

Furthermore, the Examiner cited the active area 8, depicted in Figure 1 below, of Patelmo et al. as disclosing the first active zone of the claimed invention.

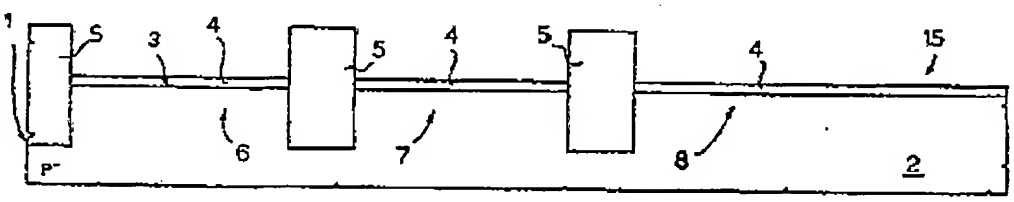

Fig1

Figure 1 of the Patelmo et al. Application

Notwithstanding the point that Figure 1 does not represent the actual device taught by Patelmo et al. but illustrates a stage of fabrication with no active components excepting some oxidation layers, the active area 8 provides the substrate where the memory transistor 74 and the selection transistor 73 are formed during fabrication.

In contrast, independent Claims 34 and 68 recite transferring, during erasure of the memory cell, charges stored in the floating gate to the first active zone. As discussed above, the memory transistor 74 comprises the tunnel oxide region 26. Although not expressly disclosed by Patelmo et al., it appears that the charge from the floating gate is transferred to the well region 22, which is implanted into another well 14, and not the active area 8 cited by the Examiner.

Consequently, for this reason also, independent Claims 34 and 68 are patentable. Their respective dependent claims, which recite yet further distinguishing features, are

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also patentable over the prior art and require no further discussion herein.

CONCLUSIONS

In view of the arguments presented above, it is submitted that all of the claims are patentable. Accordingly, a Notice of Allowance is respectfully requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number 571-273-8300 to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 this 3rd day of April, 2007.